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CARROLL, J EXAMINER

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ART UNIT	PAPER NUMBER
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2508

17

DATE MAILED: 04/04/96

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

- ☐ This application has been examined. ☒ Responsive to communication filed on 02 January 1996 ☐ This action is made final.
- A shortened statutory period for response to this action is set to expire THREE (3) month(s), 0 days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- |   |  |
|---|--|
| 1. <input type="checkbox"/> Notice of References Cited by Examiner, PTO-892.        | 2. <input type="checkbox"/> Notice re Patent Drawing, PTO-948.                   |
| 3. <input type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449.             | 4. <input type="checkbox"/> Notice of informal Patent Application, Form PTO-152. |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474. | 6. <input type="checkbox"/>  |

Part II SUMMARY OF ACTION

1. ☒ Claim(s) 17 through 42 and 44 through 66 are pending in the application.  
Of the above, claim(s) \_\_\_\_\_ are withdrawn from consideration.
2. ☒ Claim(s) 1 through 16 and 43 have been canceled.
3. ☐ Claim(s) \_\_\_\_\_ are allowed.
4. ☒ Claim(s) 17 through 42 and 44 through 66 are rejected.
5. ☐ Claim(s) \_\_\_\_\_ are objected to.
6. ☐ Claim(s) \_\_\_\_\_ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawing(s) under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawing(s) are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction(s), filed on \_\_\_\_\_, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under 35 USC 119. The certified copy has ☐ been received ☐ not been received  
☐ been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION



We have entered as Paper No. 16 the AMENDMENT filed 02 January 1996.

Due to the amendment we withdraw Claim rejections under the second paragraph of 35 U.S.C. 112 as expressed on page 4 of Paper No. 14.

Under 37 C.F.R. 1.83(a) we newly object to the Figures because they do not show every feature of the subject matter required by newly presented Claims 63 and 66. Claim 63, like Claim 42, more particularly requires a

"second polysilicon layer extends from  
the trench to a field region creating an  
electrical contact to the metal layer",

excerpted from the last four Claim lines. Figure 31B instead shows a first polysilicon layer (36) extending from a trench in the active region to a termination region where it electrically contacts metal (43a). No Figure shows the a second polysilicon layer extension as required by Claim 63. Claim 66, like Claim 45, more particularly requires a horizontal cross section of a semiconductor body to have a substantially "circular shape". No figure shows a semiconductor body having a circular shape. In response we therefore require either a showing in the Figures of the subject matter required by each of Claims 63 and 66, as excerpted *supra*, but without the introduction and further introduction of new matter prohibited under at least 35 U.S.C. 132, or we require deletion of the excerpts *supra* from the claimed subject matter.

We reject amended Claim 30, dependent Claim 31, Claim 42, and newly presented Claims 58, 59, 63 and 64 under at least the second paragraph of 35 U.S.C. 112 as being vague and indefinite. More particularly with respect to Claim 30, there is no antecedent basis for

"the exposed pattern of the second  
covering layer at the top surface of  
the third covering layer",

recited on Claim lines 39 through 41. Furthermore Claim lines 56-7 require

"junction breakdown away from the  
trench and into the.",

thus requiring a reader to speculatively discern that into which breakdown



occurs. Claim 31 is thereby vague and indefinite due to its dependency upon vague and indefinite Claim 30, discussed *supra*. Claim 58 is vague and indefinite because there are no antecedent bases for "the epitaxial region", "the epitaxial layer" and "the epitaxial layer top surface". Claim 59 is vague and indefinite thereby due to its dependency upon vague and indefinite Claim 58, discussed *supra*. Claim 63, like Claim 42, requires subject matter not originally disclosed and not originally possessed by the Applicants at the time the Invention was made. Claims 42 and 63 thereby require new matter expressly prohibited under 35 U.S.C. 132 because the subject matter claimed has no basis whatsoever in the original disclosure. We therefore additionally reject Claims 42 and 63 under the first paragraph of 35 U.S.C. 112 because they require new matter not originally disclosed. Claim 64 is vague and indefinite because there are no antecedent bases for "the gate region", "the drain region" and "the source region".

We express the following observations and opinions in response to the REMARKS on amendment pages 8 through 11.

The Applicants indicated on amendment page 9 that at least Claim 17 requires a topological distinction over the V-shaped insulated gate transistor illustrated by Tonnel in Figures 3, 6 through 12 and 14 through 19.

In response, we agree. However, we decline to overlook the fact that Tonnel further expected to alternatively form insulated gate transistors whereby the insulated gate electrode is accommodated within slots having vertical sides, evidently from the paragraph spanning columns 5 and 6. Tonnel found thereby that one would have advantageously increased packing density. Observing that Ueda et al., Reference AR provided by the Applicants on 02 July 1993, similarly found the higher packing density advantage when using insulated gate transistors whereby the insulated gate electrode is accommodated within slots having vertical sides, we thus conclude that Tonnel alternatively expected to accommodate insulated gate electrodes within slots like those shown by Ueda et al. with Figure 1.



We appreciate from amendment page 11 that the Applicants will present a terminal disclaimer when appropriate.

Not discerning a reasonable basis to conclude that the presently claimed subject matter is patentable over the alternative embodiment suggested by Tonnel, we maintain the following Claim rejections.

We reject amended Claims 17 through 22, Claims 24 through 29, amended Claims 30 and 31, amended Claims 32 through 37, Claim 44, newly presented Claims 64 and 65, amended Claims 46 through 49 and 51, amended Claims 52 and 53, and newly presented Claims 54 through 58 under 35 U.S.C. 103 as being unpatentable over considerations of Tonnel and Ueda et al., as discussed *supra*, and in the record.

We reject Claim 50 under 35 U.S.C. 103 as being unpatentable over considerations of Tonnel, Ueda et al. and Lisiak et al., Reference R of Paper No. 12, as discussed in Paper No. 12 on pages 3 through 5 therein.

We reject Claims 39 through 41 and Claims 60 through 62 under 35 U.S.C. 103 as being unpatentable over considerations of Tonnel, Ueda et al. and Yamabe et al., Reference AR provided by the Applicants on 02 July 1993. Yamabe et al. taught at least the leakage current advantage of performing etching to remove a sacrificial oxide layer to round corners of trenches accommodating insulated gate electrodes, like those anticipated by Ueda et al. and envisaged by Tonnel. We thus conclude it to have been obvious for one to have performed rounding of trenches accommodating insulated gate electrodes to gain the leakage current advantage in trench insulated gate transistors like those envisaged by Tonnel.

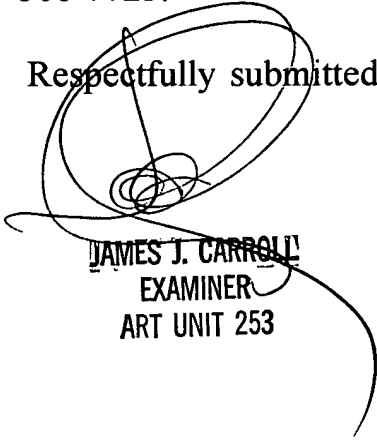
We reject Claims 17 through 42 and Claims 44 through 66 under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Patent Claim 2 and its dependent Claims in US 5,072,266, but further considered with Tonnel, Lisiak et al., Ueda et al. and Yamabe et al. teaching that differences between the claimed subject matters would have been obvious, as discussed *supra*, and in the record.



We reject all Claims.

An inquiry concerning this communication may be directed to Examiner J. Carroll at telephone number 703-308-4926 or, to the Reception Person for Group 2500 at telephone number 703-308-0956. Written communications may be received in Art Unit 2508 at FAX number 703-308-7723.

Respectfully submitted.



JAMES J. CARROLL  
EXAMINER  
ART UNIT 253